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Nanotechnologies for ICTs

Study of Silicon Nitride resonators for optomechanics and security applications

Master Thesis

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Abstract

In this work the design, fabrication and characterization of silicon nitride nano-mechanical resonators is presented, starting from silicon nitride thin films deposited on Si wafers according to ten different recipes. The properties of such devices will depend on:

- design
- material properties.

As demonstrated in the previous work [1], silicon nitride material properties (such as stoichiometry, stress, roughness, refractive index, Young's modulus) are strongly influenced by the deposition conditions (temperature, pressure, gas ratio and total gas flow).

The long term goal of this project is to achieve the highest performances in NEMS resonators, and so high quality factors, finding out the best combination between deposition condition and device design.

Most of the project is based on the microfabrication of membranes, cantilevers and beams. Two fabrications runs are performed: the purpose of the first fabrication run is to complete all the necessary trainings needed to use the tools in the cleanroom; the issues encountered during the first run are the starting point for the second fabrication run whose process flow is partially modified and optimized.

In the last part of the thesis, some measurements about cantilevers deflection are shown. These measurements are carried out by using an optical profiler providing a 3D surface profile of devices and the data are processed using the software Vision32® and Matlab®, respectively.

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1 Introduction

This chapter provides a brief description of the work carried out during this project highlighting the crucial role of nanomechanical resonators in MEMS (Micro Electro Mechanical Systems) and NEMS (Nano Electro Mechanical Systems) technologies. At the beginning, some basic definitions are given and nanoresonators are classified in three different families. The attention is also focused on the potential applications of such structures that have been extensively discussed in literature. Several techniques exist to fabricate suspended structures; some of them are discussed exploiting both advantages and limitations. After this first general description, the topic becomes more specific by analyzing the main motivations that led to choose silicon nitride as the candidate material for these devices. The last paragraph describes the contents of each chapter of the thesis.

1.1 Basic concepts

This thesis presents the fabrication of silicon nitride nano-mechanical resonators which are the basic mechanical structures for sensing and actuation in MEMS and NEMS devices. By some definitions, nano-mechanical resonators are defined to be structures with at least one dimension below the size of $1\mu\text{m}$. They can be classified in cantilevers, beams and membranes according to the support or clamp relative to the moving parts.

A cantilever is the most ubiquitous structure in the field of MEMS and consists of a singly clamped beam. Due to its ease in fabrication it has found itself in several applications including AFM (Atomic Force Microscope) tips [2], gas sensors [3], RF switches [4] or biomedical sensors [5].

A bridge is a beam that is supported on both of its ends. Due to this clamping scheme, the structure is more rigid compared to a cantilever of similar size, which also result in higher resonant frequency if used as a mechanical resonator. Doubly clamped beams are usually pre-stressed because

thin films used in microfabrication tend to have a process related tensile or compressive stress. In this case these structures are called strings.

Two-dimensional bending resonators can be divided into plates and membranes. The ideal case of a plate is reached if the mechanical behavior is dominated by the bending stiffness (flexural rigidity) of the structure. The case of a membrane occurs if there is a tensile stress inside the structure that is dominating its behavior, and the flexural rigidity does not have to be taken into account [6]. Due to its enclosed cavity, this kind of structure is suitable for a large range of applications such as mass sensors, pressure sensors, acoustic sensors and actuators in microfluidics.

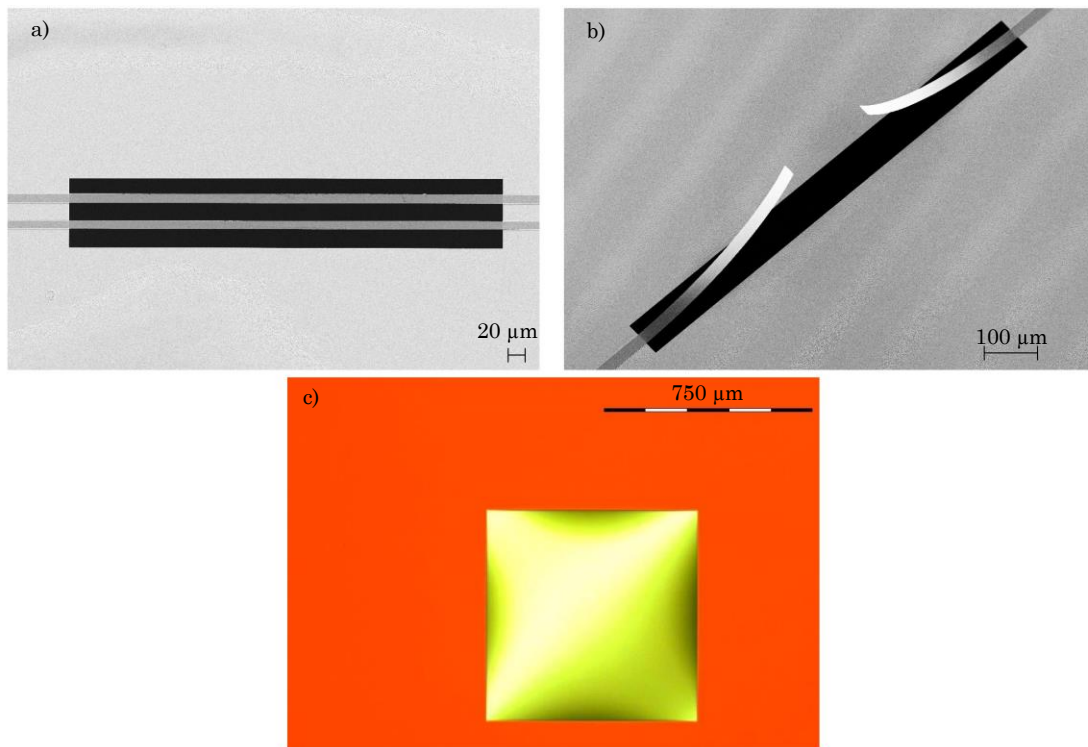


Figure 1.1 - Example of silicon nitride nanomechanical resonators fabricated at the CMi facility. a) SEM photograph of stressed nanostrings with width = 10μm, length = 500μm and thickness = 200nm. b) SEM photograph of high tensile stress nanocantilevers with width = 25 μm, length = 475μm and thickness = 200nm. c) Optical micrograph of a 750μm square SiN membrane with thickness = 200nm. It was not possible to take SEM photographs of membranes because of charge up effect.

1.2 Fabrication methods

The fabrication processes commonly used to make suspended plate structures include bulk micromachining techniques, surface micromachining techniques and wafer bonding techniques [7]. In bulk micromachining, the silicon wafer itself is viewed as the main material from which the MEMS components are made, and differs from surface micromachining where components are fabricated by deposition and etching on top of the silicon wafer, which acts as a substrate. In this project the bulk micromachining has been chosen as fabrication process.

One way to fabricate membranes using bulk micromachining techniques is the back side etch technique. In this approach the back side etch is typically achieved by silicon wet etching in a KOH bath where the etch stop layer can be provided by a heavily doped layer [8] or by the thin film deposited on the front side which will be the suspended resonator itself. The shape of the suspended plate is patterned using photolithography on the opposite surface of the wafer (i.e. its back side). Etching of silicon in KOH is highly selective along silicon crystal planes and allows precise control of dimensions only if the desired structure can be bounded by $\langle 111 \rangle$ planes, as in rectangular membranes. This could be a limitation because the integration of resonators in complex microsystems requires a greater flexibility in terms of layout.

Several variations of this technique exist, mainly differing in terms of etching process itself. For instance, a DRIE (Deep Reactive Ion Etching) process can be used to obtain a more accurate plate form because of the higher anisotropy of this etching process. The use of DRIE is really advantageous as it allows the fabrication of any-shape membranes. For example, it has been shown that DRIE process preserves both the optical quality and the mechanical quality factor of circular membranes [9].

Related to the approaches shown above is the front side etch technique for the fabrication of the suspended structures. In this way, the top side of the wafer is patterned using photolithography and then RIE techniques are used to

etch the general shape of the device. The main limitation of this technique is that devices have a tendency to be bulkier than those fabricated using surface micromachining, and the process is not suitable for CMOS industry.

1.3 Motivations¹

Resonant mechanical structures with dimensions in the micron and submicron regime offer distinct advantages over their larger mechanical and electrical counterparts in system miniaturization, power dissipation and force sensitivity. The qualitative behavior of a mechanical resonator is defined by the quality factor Q , defined as the rate with which a resonators dissipates energy. It is typically defined as:

$$\frac{1}{Q} = \frac{\Delta f}{f_0} \quad (1.1)$$

where f_0 is the resonant frequency and Δf is the full width at half power of the resonance peak. The resonance frequency of a micro- or nanomechanical resonator is typically close (slightly lower) to the eigenfrequency of the same system assumed without losses. The eigenfrequency can be evaluated by means of analytical continuum mechanical models or FEM (Finite Element Modelling) simulations.

Increasing the quality factor is advantageous for several applications: for example, in resonant sensors high Q enables better resolution, and in optical cavities it reduces the resonator optomechanical coupling to the environment. Silicon nitride micro- and nanomechanical resonators are a good candidate for achieving high quality factors Q s. Furthermore, some experiments [10] comparing resonators made of differently stressed silicon nitrides verify that the higher stress devices have the highest quality factors for a wide range of frequencies. The stress in silicon nitride thin films is a important property which can be manipulated by varying the deposition parameters.

¹ This paragraph is strongly based on Reference [6].

Despite the continuous effort to optimize the quality factor of SiN resonators, it remains important to understand what are the most limiting sources that contribute to damping mechanisms. At the resonant frequency the energy is commuting between kinetic and potential energy. In a lossless mechanical structure, the total energy in the mechanical system is passed back and forth endlessly between kinetic and potential energy while in a real structure a little part of the energy is lost during every cycle of vibration due to damping mechanisms. Different sources of energy loss can be found in nanomechanical resonators so that the total quality factor can be written as the sum of different dissipation mechanisms:

$$\frac{1}{Q} = \frac{1}{Q_{medium}} + \frac{1}{Q_{clamping}} + \frac{1}{Q_{intrinsic}} + \frac{1}{Q_{other}} \quad (1.2)$$

where Q_{medium} stands for all losses due to the interaction of the mechanical structure with a fluidic or ballistic medium, $Q_{clamping}$ are losses from energy radiating into the environment over the physical clamping sites of the resonator, $Q_{intrinsic}$ summarizes all dissipation mechanisms happening within the resonator both in bulk and on surface and, Q_{other} sums up loss mechanisms such as *electrical charge damping* caused by charges trapped on the resonator or *magnetomotive damping* which results from electrical dissipation in resistive elements due to Eddy currents induced by an external magnetic field [11].

1.4 Thesis guideline

On the basis of what has been said, mechanical resonators are fabricated using the deposited layers of silicon nitride by bulk micromachining. The long term goal of the project is to measure the quality factor of said resonators so that internal losses can be characterized.

The thesis is organized in four chapters. The second chapter entitled “Design and fabrication process”, provides the description of the devices design and gives a detailed analysis of the two fabrication runs. The third chapter

entitled “Characterization”, contains the theoretical basis of measurements, the analysis of the processed data and the experimental setup of this study. The last chapter is entitled “Conclusions” and is devoted to a summary of the main results obtained from the project and to perspectives regarding the future work.

2 Design and fabrication process

The purpose of this chapter is to describe in detail all the steps involved in the microfabrication of nano-resonators discussed in the previous chapter. Two fabrication runs will be discussed with similar structures. The first part will describe the process flow and the design of the masks highlighting the motivations that have brought appropriate choices. The subsequent sections will describe the issues encountered during the fabrication and the results achieved at the end of the process.

All the steps of the process flows are performed according to the recipes used at the Center of MicroNanotechnology (CMi) facility at Ecole Polytechnique Fédérale de Lausanne (EPFL). Detailed run sheets and recipes can be found in Appendix A.

2.1 First fabrication run

The main aim of the first fabrication run is primarily to reach the end of the process flow and complete all the necessary trainings needed to use the tools in cleanroom. The issues faced during the process and discussed in Section 2.1.4 will be the starting point for the implementation of the second fabrication run. The detailed run sheet for this fabrication is illustrated in Table A.1.

2.1.1 Process flow

In this section the process flow of the first fabrication run will be discussed in detail. The first devices are fabricated on a Ø100mm Single Side Polished (SSP) <100> p-type test wafer (0.1-100Ωcm) with 200nm of LPCVD Silicon Nitride (Si₃N₄) deposited on both sides.

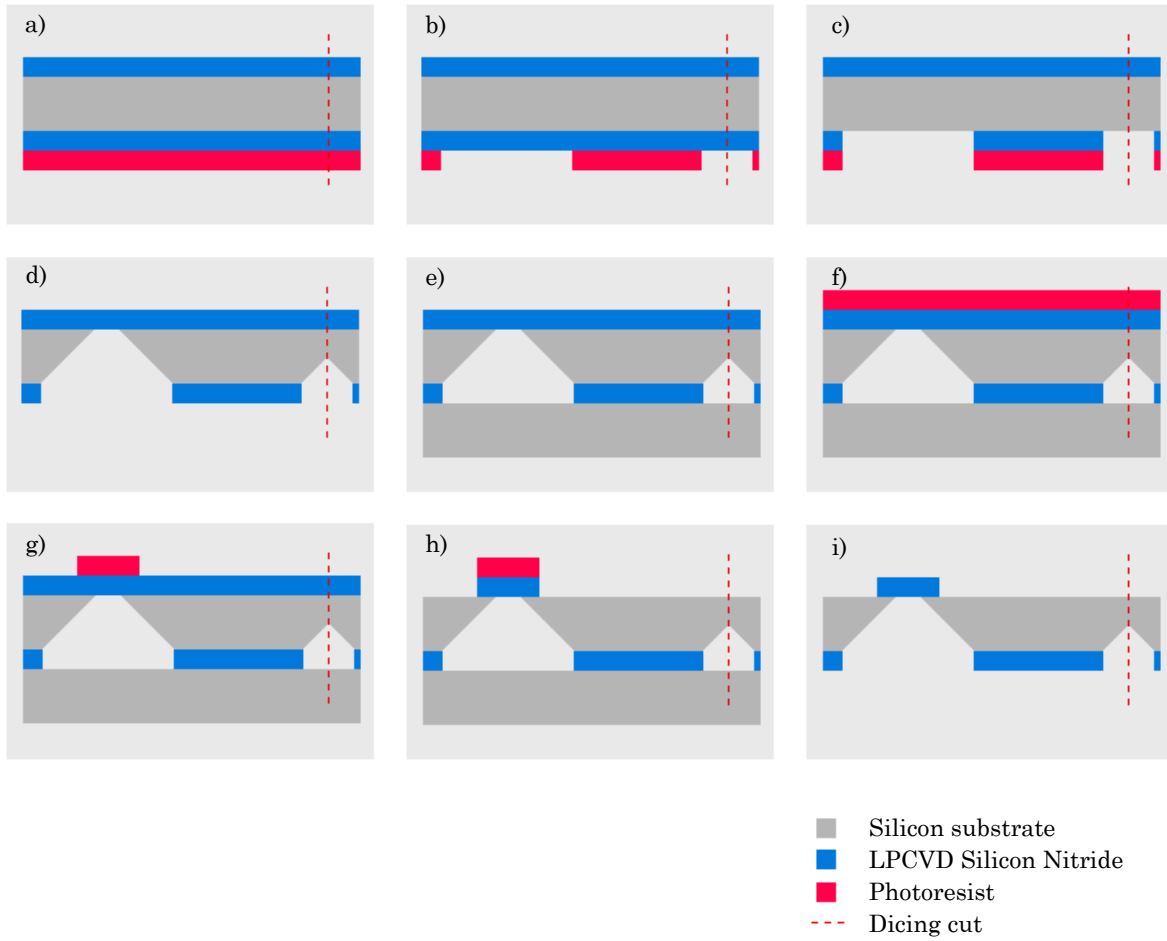


Figure 2.1 - First fabrication run process flow. For the sake of simplicity the schematic cross section for the fabrication of a membrane is represented. The red dashed line virtually divides two adjacent chips on the same wafer.

As shown in Figure 2.1, the devices are realized through two lithography processes. The first one is performed to define windows in the back side of the wafer [Fig. 2.1b]. The back side of the wafer is coated with a $1\mu\text{m}$ thick photoresist layer and then exposed by direct laser writing optical lithography. The back side silicon nitride layer is etched by Reactive Ion Etching (RIE), using fluorine chemistry, and it acts as a hard mask during KOH etch [Fig. 2.1c]. After the resist strip using wet chemistry, the wafer is plunged into the 23% KOH bath at 90°C where silicon anisotropic etching occurred up to reaching the silicon nitride layer or stopped by the slow etching $\langle 111 \rangle$ planes in the silicon [Fig. 2.1d]. The previous parameters have been selected by CMI

facility to optimize etching with a minimum of roughness. At this point, the wafer is too fragile to be directly subjected to the front side lithographic steps, consequently, it is stuck on a dummy wafer by using a wax called QuickStick135 [Fig. 2.1e]. This thermoplastic polymer can be applied manually by using an hot plate heated at 135°C . Then, a second lithography step takes place on the top side of the wafer. In this case, the front side pattern is obtained by mask alignment with the back side one [Fig. 2.1g]. More details on mask designs and fabrication will be discussed in the next paragraphs.

The resulting resonating devices are obtained from the top silicon nitride layer etched by RIE and the remnant photoresist is stripped in an oxygen plasma.

To separate the wafers, the assembly is just heated again on the contact hot plate at 135°C and QuickStick135 is cleaned in acetone [Fig. 2.1i]. The last step, before releasing the final chips, is the wafer dicing. It occurs by simply breaking the wafer along the ‘dicing lines’ without the use of a dicing saw that could damage so fragile structures.

2.1.2 Masks design

The mask design is described starting from the elementary building blocks which are then gathered into chips and wafers. According to the process flow, only two lithography steps are needed, for patterning the back side and the front side. All masks designs are drawn using L-Edit software.

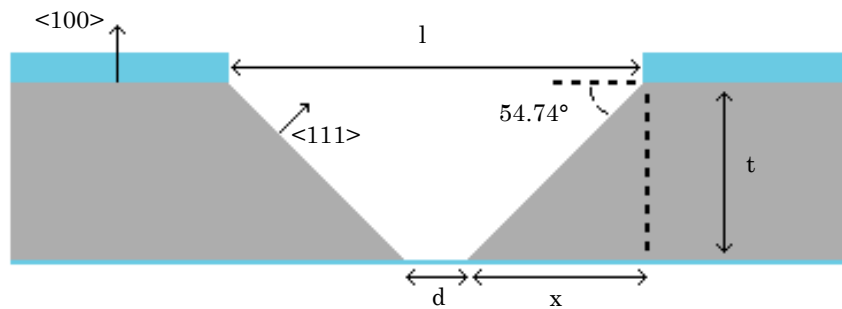


Figure 2.2 - Typical V-shaped groove in (100) silicon wafer.

Back side mask

The back side pattern is designed to define the apertures on the bottom of the wafer. The dimensions of such apertures are strictly related to the geometrical size of the devices and are calculated taking into account that KOH etch is anisotropic, so the silicon etch rate depends on the crystallographic planes.

In the most general case, to reproduce the lateral length d on the top side of the wafer, the corresponding aperture length l in the back side should be:

$$l = d + 2 \cdot t \cdot \tan(90^\circ - 54.74^\circ) \quad (2.1)$$

where t is the etch depth. It can be deduced that the etch depth at the end of the process can be directly controlled by the dimensions of the window on the back side: this principle is used to get the ‘dicing lines’. In particular, these lines are patterned so that only half of the whole wafer thickness is etched; this choice is due to the fact that the residual silicon thickness must be sufficiently thick to prevent the dicing before the end of the process and at the same time so thin to allow chips separation without damage.

The back side mask design is very simple. Chips are designed to be 10mm x 10mm and each of them can contain twenty rectangular or sixteen square apertures [see Fig. 2.3]. For each kind of device many different dimensions needed to be explored: for rectangular windows the width is kept fixed and the length is varied while for the square ones both the sizes are varied. All the possible membranes dimensions are listed in the table below.

Rectangular membranes	Square membranes
75x250	250x250
75x500	500x500
75x750	750x750
75x1000	1000x1000

Table 2.1 - Different membranes dimensions expressed in μm . These numbers are not related to the back side apertures dimensions but refer to the effective membranes dimensions.

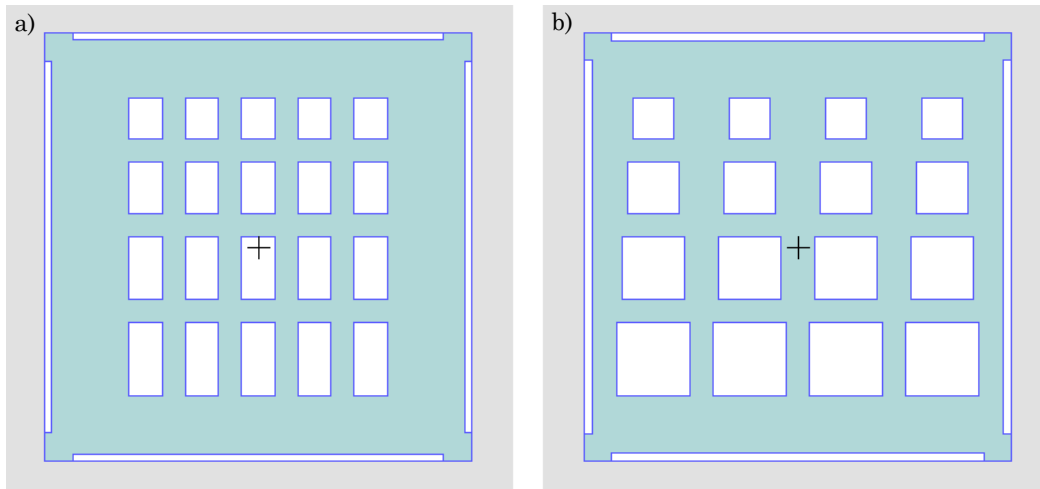


Figure 2.3 - Back side masks for two different chips. On both pictures the dicing lines apertures can be observed at the outline of each chip. The minimum distance between any two adjacent apertures is 500 μ m. (a) Rectangular apertures of different lengths for the fabrication of cantilevers or beams. (b) Square apertures for the fabrication of membranes.

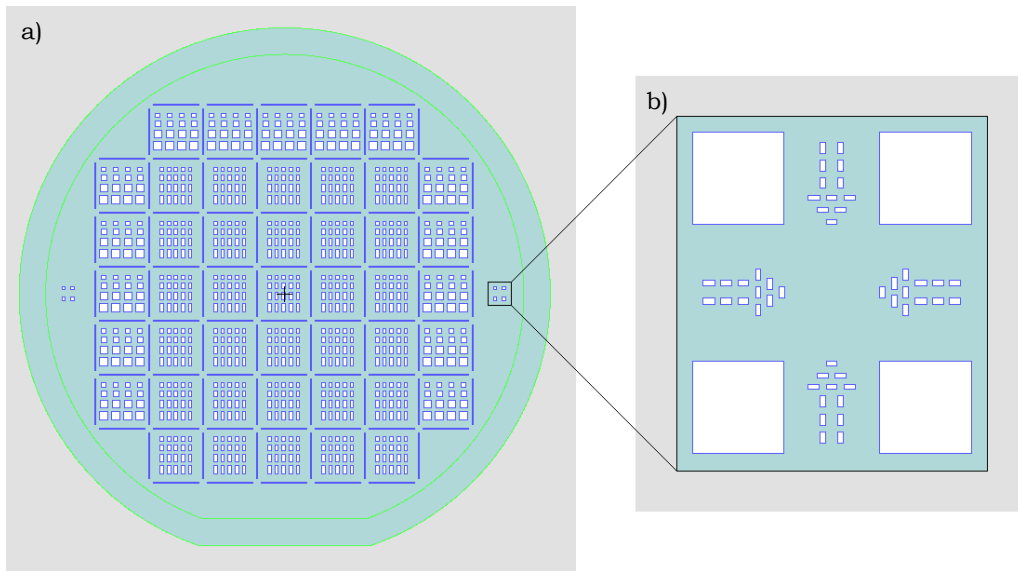


Figure 2.4 - (a) Back side mask of the Ø100mm wafer. (b) Zoom in of the alignment marks.

Figure 2.4a shows how the chips presented so far are organized into the final wafer design. There are three types of 10mm square chips containing cantilevers, beams and membranes, respectively. There are forty-five chips on a Ø100mm wafer, fifteen of each type. The chips containing membranes are

placed in the outer region of the wafer since they are more susceptible to break during the front side spin-coating, resulting in a bad lithographic process on a wider area which reduces the yield. In Figure 2.4b the alignment marks for the front side mask alignment are shown.

Front side mask

The front side pattern, differently from the back side one, is reproduced on a chromium mask whose fabrication details will be discussed in Section 2.1.3. The front side mask is designed in a such a way to adjust, in the same chip, cantilevers or beams of different lengths and widths. The values chosen for the width are $50\mu\text{m}$, $25\mu\text{m}$, $10\mu\text{m}$, $5\mu\text{m}$ and $2\mu\text{m}$ while the length can assume the values listed in Table 2.1.

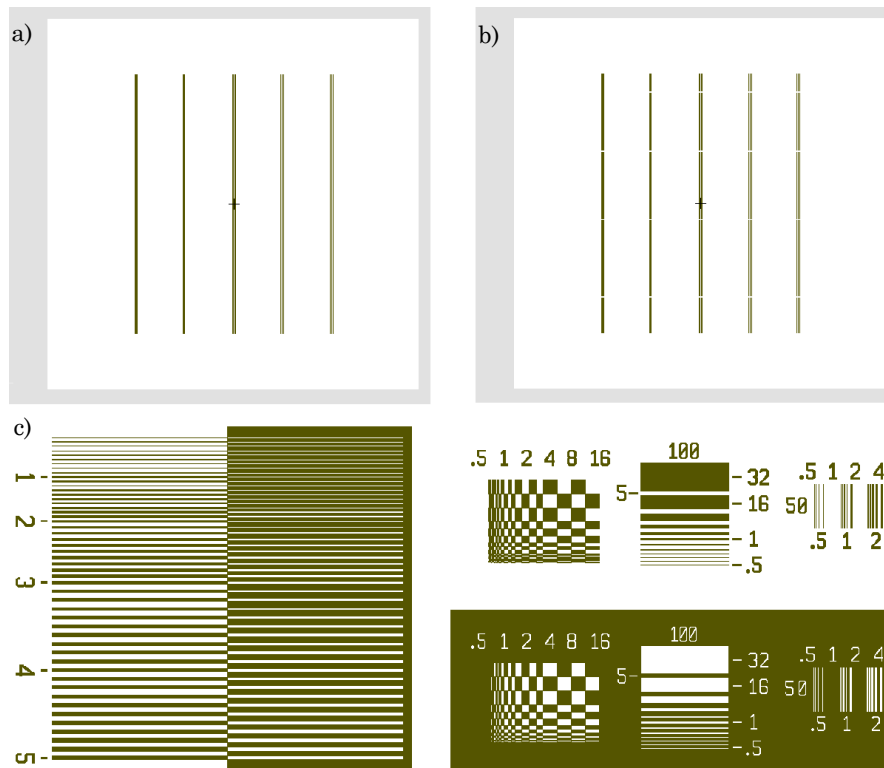


Figure 2.5 - (a) Front side pattern for the chip containing beams. (b) Front side pattern for the chip containing cantilevers. (c) Exposure grid for exposure tests and for lithography quality check on the processed wafer. [13]

2.1.3 Front side mask fabrication

The process flow of the mask fabrication is illustrated in Figure 2.6.

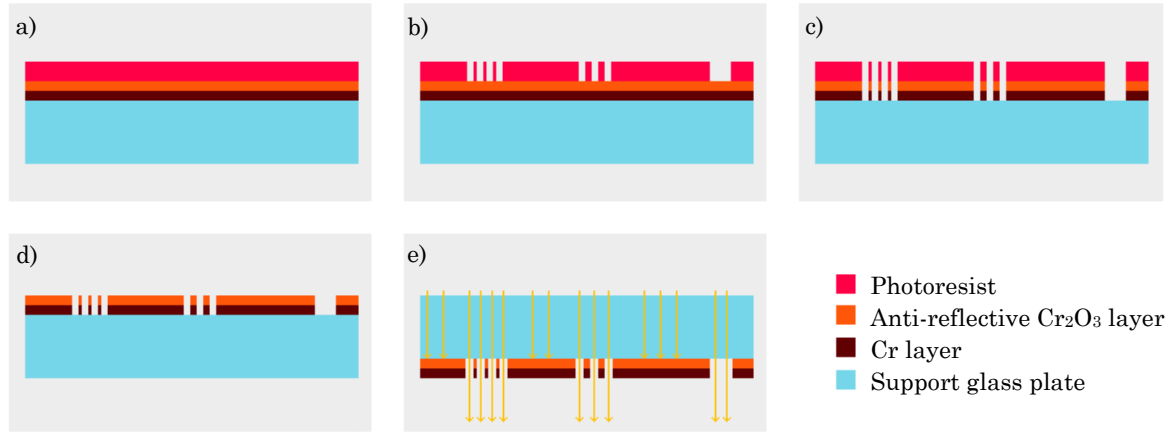


Figure 2.6 - Process flow of the mask fabrication.

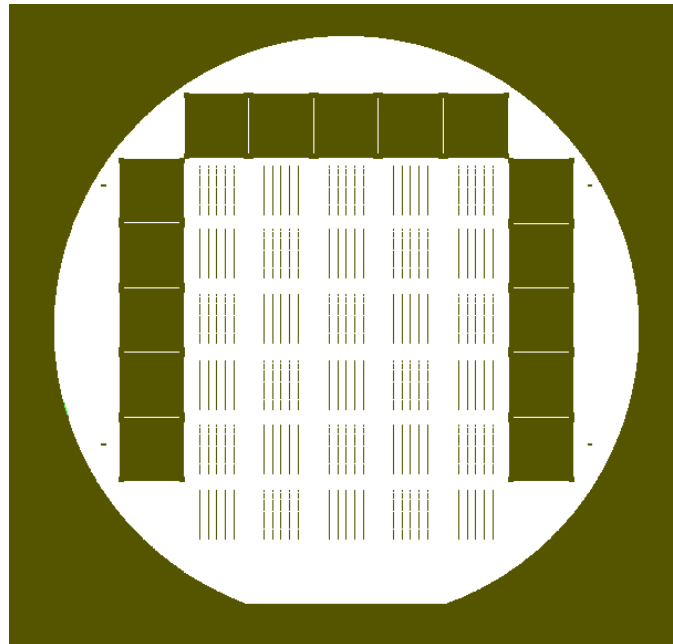


Figure 2.7 - Chromium mask for the front side design.

The starting material is a 5"x5" chrome blank mask whose specifications can be found in the Data Sheet available on the CMi website [12]. The photoresist layer is exposed, according to designed pattern, by direct laser writing optical

lithography and then developed [Fig. 2.6b]. The chromium blank and the anti-reflective Cr_2O_3 layer are etched for 90s in a Cr-etch bath at 20°C [Fig. 2.6c]. After a fine rinse, the mask is plunged in Technistrip bath for resist strip and then rinsed and dried again [Fig. 6.2d]. At this point the mask is ready to be used noticing that the image of the written data is mirrored over the y-axis [Fig. 2.7]. The detailed run sheet for this fabrication is shown in Table A.3.

2.1.4 Issues encountered and solutions

Scratches on the Si_3N_4 top layer

The first problem encountered during the first fabrication run is the scratching of the silicon nitride top layer. This issue is mainly caused by the direct physical contact between the top side silicon nitride thin film and the wafer holder, whose function is to clamp the wafer by a vacuum process during spin-coating, exposure and development of the back side. A scratched layer adversely affects device properties and the yield of the process, as shown in Figure 2.8. The best solution adopted is to introduce a protective layer: an amorphous silicon layer of 200nm is deposited, since the last can easily be removed in the KOH bath. This additional step will be the starting point of the second fabrication run process flow.

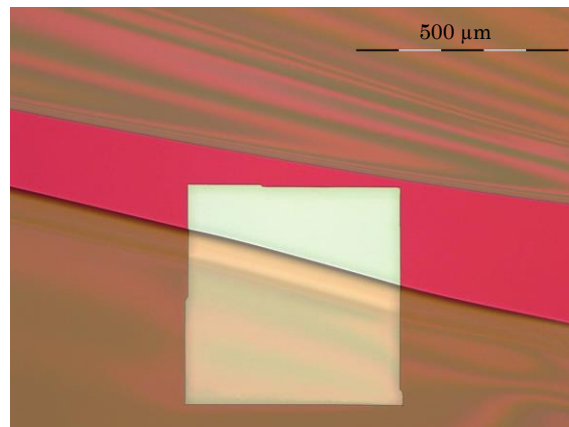


Figure 2.8 - Optical micrograph after front side spin-coating. The coating is not uniform due to surface irregularities introducing a lowering in yield.

Membranes indentations

The mechanical properties of anisotropically etched membranes can be degraded by surface texture effects: inhomogeneities formed during the KOH etch may extend to the bottom of the cavity, thereby deforming the edges bounding the structure. A ‘slate-like’ appearance of side-walls [Fig. 2.9a], etched in a SSP $\langle 100 \rangle$ test wafer in aqueous 23% KOH solution at 90°C, is observed. The wafer under analysis is covered on both sides with 200nm of LPCVD High Stress silicon nitride.

A number of possible causes are investigated to discover the origins and to avoid the formation of this effect. First of all, the side-wall quality dependence on the back side roughness is analyzed; only a minor influence is noted passing from single- to double-side polished wafers with high stress silicon nitride [Fig. 2.9b]. According to a previous study [14], such surface defects are primarily caused by wafer stress, introduced during the high-temperature LPCVD of the silicon nitride layer, and possibly enhanced by the presence of dislocations. The latter form sites which will be etched more quickly and thus create micro-pits in the $\{111\}$ planes; these pits grow outward within the affected $\{111\}$ planes to form the indentations observed. The formation of such irregularities can be also examined through an atomic-scale model [15]. On the basis of these results, a DSP $\langle 100 \rangle$ wafer with low stress LPCVD silicon nitride is etched in KOH aqueous solution at 90°C and this time no indentations appeared [Fig. 2.9c]. At this point, it is verified that the irregularities were also influenced by the temperature of the etch bath; more precisely, the temperature is lowered to 60°C at which correspond a KOH concentration of 40%, according to the recipe recommended by CMi facility. As shown in Figure 2.9d, a lower temperature process has brought significant improvements to this issue, being all imperfections disappeared. The unwanted consequence of this choice is the reduction of the etch rate of about six times, from $\sim 120\mu\text{m/h}$ to $\sim 20\mu\text{m/h}$, which is not a viable option for high-volume production. This is the main reason for which the process flow of the second fabrication run is partially revised.

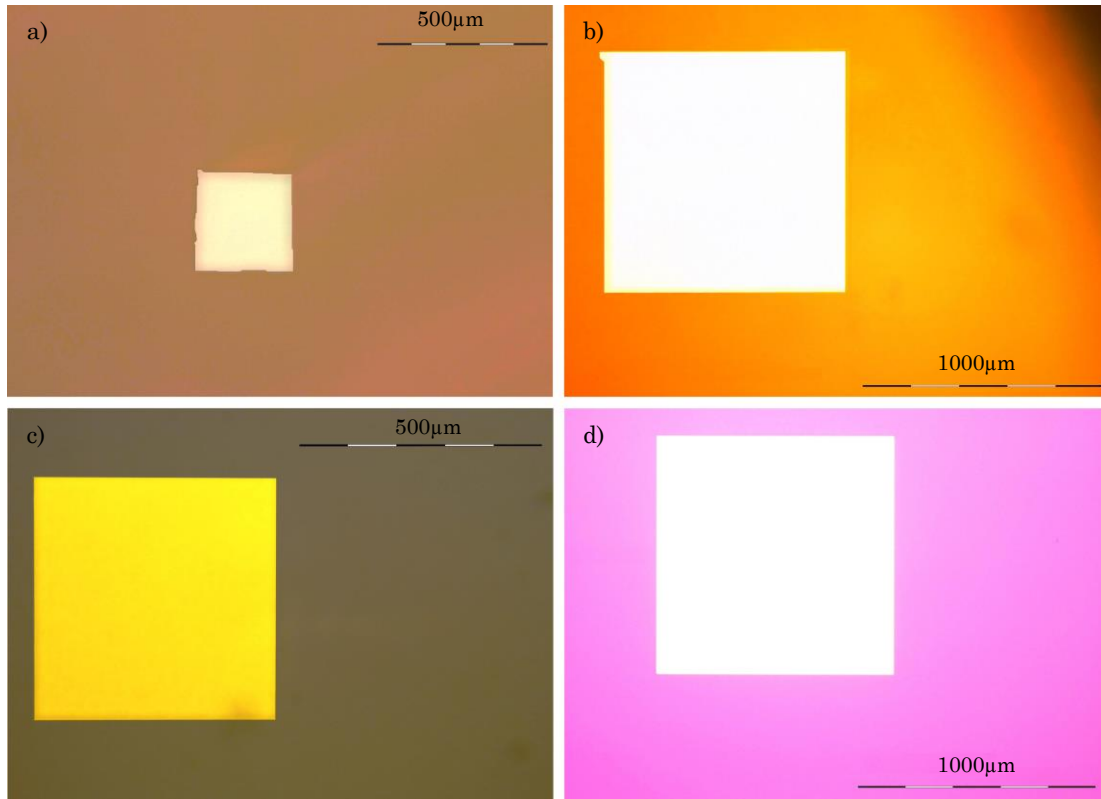


Figure 2.9 - a) Picture of a 250µm square membrane in high stress silicon nitride, fabricated with 23% KOH at 90°C in a SSP wafer. Several indentations appeared at the borders of the membrane, whose thickness varies from few µm up to 15 µm. This effect causes an oversizing of the membrane. b) Picture of a 1000µm square membrane in high stress silicon nitride, fabricated with 23% KOH at 90°C in a DSP wafer. There is an improvement with respect to the previous case, but some evident indentations still appear (in the top left corner). c) Picture of a 500µm square membrane in low stress silicon nitride, fabricated with 23% KOH at 90°C in a DSP wafer. No indentations appeared. d) Picture of a 1000µm square membrane in high stress silicon nitride, fabricated with 40% KOH at 60°C in a DSP wafer. The borders are well defined and irregularities went away.

2.1.5 Results

In this paragraph the results obtained from the first process flow will be discussed focusing in particular on the yield of the process. It is important to underline that yield is intended as the number of broken squared membranes, without including those which are not releasable due to indentations discussed in the previous paragraph. The attention is mainly focused on membranes as

these are more likely to break due to more extended free-standing surfaces. A quantitative statistic is carried out and results are listed in Table 2.2.

	High Stress DSP wafer (23% KOH at 90°C)	Low Stress DSP wafer (23% KOH at 90°C)	High Stress DSP wafer (40% KOH at 60°C)	Low Stress DSP wafer (40% KOH at 60°C)
KOH etching	0	0	2	0
Neutralization	2	0	2	0
QuickStick135	2	0	2	0
Front side spin- coating	4	2	5	1
Mask alignment and exposure	16	3	5	1
Development	16	3	6	2
Si ₃ N ₄ dry etching	16	3	6	3
Photoresist strip	16	3	6	3
Yield	~93%	~99%	~98%	~99%

Table 2.2 - Broken square membranes statistics after each step of the process flow.

In the table above, the processed wafers are placed in columns according to the chronological order of fabrication, so the first wafer which has been processed is in the first column. For the first wafer, it is observed that the yield is lowered after mask alignment and exposure because of the ‘contact mode’ option: in this case the mask is pressed chrome-side down against the resist-coated wafer during the exposure. Ideally, the gap between mask and wafer goes to zero, which minimizes diffraction effects. A reasonable improvement is obtained, for the other wafers, switching to ‘proximity mode’ where a small separation between mask and wafer is introduced and controlled by a constant nitrogen flow. The resolution achieved is still sufficient for the exposure of the most critical dimension which is 2 μ m [Fig. 2.10a].

The last remark emerging from data analysis is that the yield is dependent on the intrinsic stress in silicon nitride thin films: higher is the stress, the lower is the yield.

2.1.6 Summary and conclusion

The first fabrication run has revealed several issues related to both devices reliability and yield. The most important between them is the indentations appearance which is discussed in Paragraph 2.1.4 and whose solution led to a consistent etch rate reduction. This choice is experimented on DSP wafers (thickness: 380 μm) but is not suitable (from a large-scale production point of view) for SSP wafers (thickness: 525 μm), because in this way just the KOH etch should last more than 26 hours. Consequently, the process flow must be modified in order to be adapted to SSP wafers.

Nevertheless, at this step, the yield was higher than expected and some measurements could be performed on such devices. Some of them are illustrated in Figure 2.10.

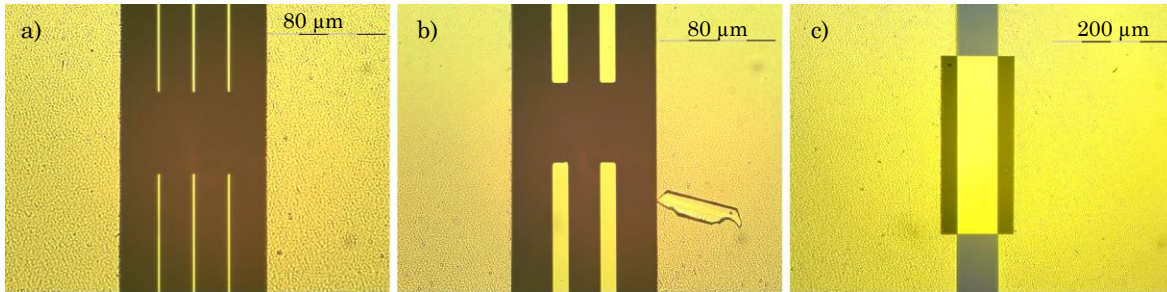


Figure 2.10 - Some optical micrographs of high stress silicon nitride devices. a) Cantilevers of dimensions: length = 100 μm , width = 2 μm , thickness = 200nm. b) Cantilevers of dimensions: length = 100 μm , width = 10 μm , thickness = 200nm. c) Beam of dimensions: length = 250 μm , width = 50 μm , thickness = 200nm.

2.2 Second fabrication run

The second fabrication run is carried out on the basis of what was discussed in the previous section. The goal is to get the best process flow in terms of yield and quality of devices. The fabrication runs are very similar except for two additional steps: front side silicon sputtering as protective layer and silicon anisotropic dry etching before KOH etching. Despite this, the mask design for the back side has not undergone major changes while the mask for the front side is compatible with the new process and is reused.

In this section, the attention will be more focused on the additional steps while the rest can be considered similar to what was discussed in Paragraph 2.1. The detailed run sheet of this fabrication run is presented in Table A.2.

2.2.1 Process flow

The process flow of the second fabrication run is presented in Figure 2.11. The fabrication is performed on a Ø100mm Single Side Polished (SSP) <100> p-type test wafer (0.1-100Ωcm) with 200nm of LPCVD Silicon Nitride deposited on both sides.

The first step is to deposit on the front side of the wafer a 200nm film of amorphous silicon [Fig. 2.11a]. As discussed in the previous section, the layer will protect the front side silicon nitride layer from scratches during the lithographic steps performed on the back side. This time, the back side of the wafer is coated with a thicker photoresist layer of 5μm, because of the PR mask selectivity during the anisotropic dry etch of silicon. A overnight bake at 80°C is then necessary to improve the thermal stability of the photosensitive resist. As previously, the back side silicon nitride layer is etched by RIE [Fig. 2.1d]. At this point, the way the silicon substrate is etched changes as follows: assuming a thickness of 525μm for a SSP wafer, a depth of 425μm is etched by DRIE (Deep Reactive Ion Etching or Bosch etch) while the remnant 100μm frame is etched into the 40% KOH bath at 60°C. Bosch etch is a pulsed SF₆/C₄F₈ process

in which silicon is etched in a fast but isotropic fashion during SF_6 pulse, and C_4F_8 pulse is used to passivate the sidewalls of the etched features. The recipe used at the CMi facility is optimized for big apertures (typically more than $50\mu\text{m}$) and to minimize the side-walls roughness. The expected geometry for the trenches is shown in Fig. 2.11f.

To avoid redundant information, all the steps regarding the front side processing are omitted, as they are identical to those of the first fabrication run discussed in Paragraph 2.1.1..

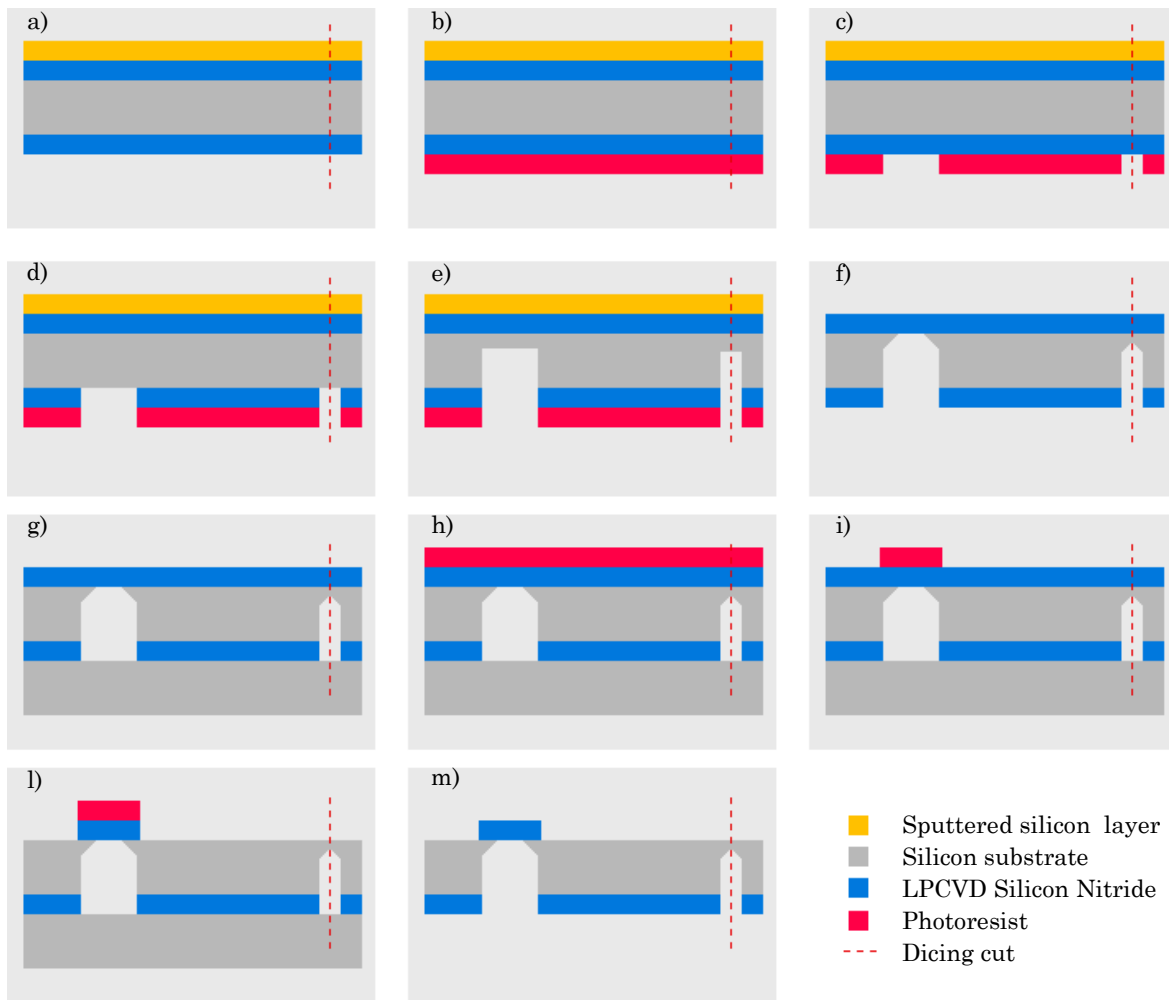


Figure 2.11 - Process flow for the second fabrication run.

2.2.2 Mask design

In this paragraph the mask design will be discussed focusing mainly on the back side pattern while the front side one is left as it was. The changes are related to the back side apertures dimensions because the geometry of the etch process is varied with respect to the first fabrication, as shown in Fig. 2.12.

Equation 2.1 can be reused to determine the membrane lateral lengths where the thickness t is no longer that of the whole wafer but the remnant silicon frame after DRIE to be etched in the 40% KOH solution at 60°C. Thus, according to the calculations, any length of the back side opening is obtained by adding 140 μm to the corresponding membrane length; for instance, a square membrane of 250 μm corresponds to a square aperture on the back side of 390 μm .

It can be noticed that the membrane size is strictly related to the thickness t which is a great limit to the process, since the etched depth is not easily controllable. In fact the etch rate per cycle during Bosch etch is a complex function of the polymer deposition rate, the polymer etch rate and the silicon etch rate [16].

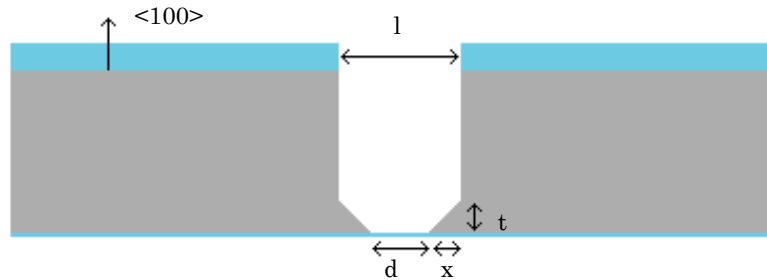


Figure 2.12 - Cavity profile after Bosch etch followed by wet etch in 40% KOH solution.

2.2.3 Issues encountered

ARDE effect

DRIE introduces new issues related to the so called ARDE effect (Aspect Ratio Dependent Etch). Due to this phenomenon, the etch rate is limited by the transport of etch species to the bottom of the trenches and of etch products out

of them. As a consequence, the etch rate decreases as the AR (Aspect Ratio) is increased. The aspect ratio is defined as the mathematical ratio between the depth and the width of the trench.

In the case under analysis, this effect could be extremely relevant since the dimensions of the apertures on the back side vary in a range of about 900 μm . The influence of ARDE is quantified by measuring the trenches depth during the etching by using Veeco Wyko NT1100, an optical profiler providing 3D surface profile measurements without contact [17]. The VSI (Vertical Scanning Interferometry) mode allows to measure steps up to 1mm high. The basic interferometric principle is the following: light reflected from a reference mirror combines with light reflected from a sample to produce interference fringes, where the best-contrast fringe occurs at best focus. The interferometric objective moves vertically to scan the surface at varying heights. As the system scans downward, an interference signal for each point on the surface is recorded. The measurements, recorded for three steps of 15 minutes during DRIE, are reported in Table 2.3 and Table 2.4.

Aperture dimensions ($\mu\text{m} \times \mu\text{m}$)	After 15'	After 30'	After 45'
215 x 390	158 μm	298 μm	424 μm
215 x 640	159 μm	298 μm	428 μm
215 x 890	159 μm	299 μm	429 μm
215 x 1140	158 μm	299 μm	431 μm
390 x 390	159 μm	295 μm	430 μm
640 x 640	161 μm	300 μm	430 μm
890 x 890	160 μm	301 μm	438 μm
1140 x 1140	160 μm	301 μm	440 μm

Table 2.3 - Etch depths for different apertures measured every 15 minutes.

Aperture dimensions ($\mu\text{m} \times \mu\text{m}$)	0' - 15'	15' - 30'	30' - 45'
215 x 390	10.53 $\mu\text{m}/\text{min}$	9.33 $\mu\text{m}/\text{min}$	8.4 $\mu\text{m}/\text{min}$
215 x 640	10.6 $\mu\text{m}/\text{min}$	9.27 $\mu\text{m}/\text{min}$	8.67 $\mu\text{m}/\text{min}$
215 x 890	10.6 $\mu\text{m}/\text{min}$	9.33 $\mu\text{m}/\text{min}$	8.67 $\mu\text{m}/\text{min}$
215 x 1140	10.53 $\mu\text{m}/\text{min}$	9.4 $\mu\text{m}/\text{min}$	8.8 $\mu\text{m}/\text{min}$
390 x 390	10.6 $\mu\text{m}/\text{min}$	9.07 $\mu\text{m}/\text{min}$	9 $\mu\text{m}/\text{min}$
640 x 640	10.73 $\mu\text{m}/\text{min}$	9.27 $\mu\text{m}/\text{min}$	8.67 $\mu\text{m}/\text{min}$
890 x 890	10.67 $\mu\text{m}/\text{min}$	9.4 $\mu\text{m}/\text{min}$	9.13 $\mu\text{m}/\text{min}$
1140 x 1140	10.67 $\mu\text{m}/\text{min}$	9.4 $\mu\text{m}/\text{min}$	9.27 $\mu\text{m}/\text{min}$

Table 2.4 - Etch rates evaluated for each time interval, showing how ARDE effect affects the etching process.

The data reported in the previous tables confirm the significant influence of the ARDE effect (see Figure 2.13). In fact, apart for the case of 640 μm square aperture, whose etch rate is not expected to be so low in the last 15 minutes, the etch rate for larger apertures seems to be higher with respect to smaller ones. This leads to a not uniform distribution of etch depths for different apertures, keeping in mind that the target depth after 45 minutes should be 425 μm . Since the ARDE effect is most critical for the smallest rectangular aperture, approaching as close as possible to the target depth involves the over-etching of larger apertures. The over-etching which can range from 5 μm to 15 μm , influences the membrane lateral lengths because the etched silicon thickness during KOH etch is less than expected causing a membrane oversizing.

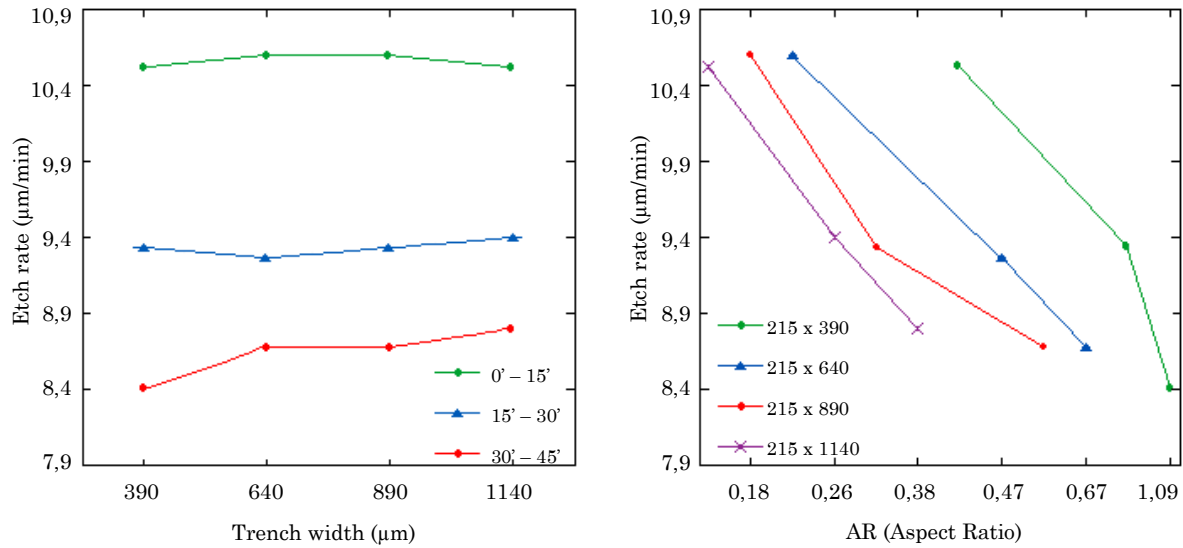


Figure 2.13 - a) Etch rate vs trench width for rectangular membranes with a common length of 215 μm. The etch rate values are plotted for each time interval of 15 minutes. During the first 30 minutes of the Bosch process the etch rate is almost constant for different aperture size, so ARDE can be neglected. In the last time interval (30'-45', red curve), the ARDE influence starts to be significant because the etch rate difference between the smallest width and the largest one is about 0.5 μm. This difference is not irrelevant since it causes an etch depth difference of about 7 μm in 15 minutes. b) Etch rate vs Aspect Ratio for rectangular membranes. The AR values on the x-axis are evaluated after each step of 15 minutes as the ratio between the etched depth and trench width. According to the ARDE effect, the etch rate decreases as the Aspect Ratio increases and, this effect occurs prior for the smallest aperture (green curve).

Dicing lines

ARDE can prove advantageous for the dicing lines fabrication because the etch depth can be controlled by choosing an appropriate width. By virtue of this, it is possible to avoid any further increase of complexity to the back side mask design. After some experimental tests on the dicing lines toughness, their width was designed to be 50 μm.

Alignment marks

Another issue introduced by ARDE effect is related to the alignment marks that consist of four 50 μm square membranes placed in diametrically opposite

regions on the wafer [Fig. 2.4b]. The corresponding $190\mu\text{m}$ square apertures on the back side are strongly affected by ARDE, in fact their depth after 45' of DRIE is measured to be $370\mu\text{m}$. This value differs by $55\mu\text{m}$ from the predicted depth ($425\mu\text{m}$) and so the 'alignment membranes' after the 40% KOH etch did not appear. Actually, this effect is also strongly enhanced by the fact that the Bosch process etch rate is not uniform: the etch rate is lower in the peripheral part of the wafer. However, the problem is exceeded by performing the alignment directly on two diametrically opposite chips, a choice that has led to optimal results.

2.2.4 Results

As widely discussed in the previous paragraph, the main limitation of the second fabrication run process flow is related to a good control of membranes size. Despite this, the process is improved compared to the previous one in terms of devices quality, since issues encountered during the first fabrication run such as indentations and surface scratching are definitively solved. Therefore, the goals of the second fabrication run are successfully fulfilled.

On the basis of these positive outcomes, the optimized process flow is reproduced on eight wafers; these wafers are covered on both sides, by a LPCVD silicon nitride layer according to eight different recipes obtained by manipulating four parameters during the SiN deposition: temperature, pressure, gas ratio $\text{SiH}_2\text{Cl}_2/\text{NH}_3$ and total gas flow [1]. The fabrication has produced a large family of devices for each wafer, so that a good characterization of their properties can be carried out.

2.2.5 Conclusion

From the comparison between the two fabrication runs it is clear that the second process flow has brought considerable improvements in terms of devices quality. However, a better quality of devices is obtained by losing the optimal

control on their size, so on their intrinsic properties because, for instance, the eigenfrequencies of a membrane depend on the side lengths L_x and L_y [6].

3 Characterization

In this chapter the first step toward the characterization of silicon nitride devices is presented. Several measurements are performed to characterize the cantilevers deflection induced by the intrinsic stress of the silicon nitride thin film. The deflection of micro-cantilevers is measured by the optical interferometry method and data are processed by using Vision32® and Matlab® software, respectively.

3.1 Thin film stress

Thin films are found to be integral parts in NEMS and MEMS which are designed to serve as sensors and actuators. During the deposition process, the thin film may acquire a residual stress that can be either compressive or tensile. Typically, for LPCVD nitride layers the measured stress is tensile.

Measured stress can be separated in three additive components: thermal stress, intrinsic stress and a third stress component related to a boundary or interfacial layer [18].

$$\sigma_m = \sigma_{th} + \sigma_i + \sigma_{bl} \quad (3.1)$$

The residual stress σ_m in thin films induces wafer bow as illustrated in Figure 3.1. The contribution of the boundary layer stress to wafer bow can be neglected if the thickness of the bulk layer is large enough compared to that of the interfacial layer. In this case Eq. 3.1 can be rewritten as:

$$\sigma_m = \sigma_{th} + \sigma_i \quad (3.2)$$

Thermal stress arises when wafers are cooled from process to measurements temperature and is due to the difference in thermal expansion coefficients between film and substrate. It is calculated as:

$$\sigma_{th} = \int \frac{E_f}{1 - \nu_f} \cdot (\alpha_{Si} - \alpha_{Si_3N_4}) dT \quad (3.3)$$

where E_f and ν_f are the Young's modulus and the Poisson's number of the thin film, α_{Si} and $\alpha_{Si_3N_4}$ are the thermal expansion coefficients for silicon and silicon nitride and, T is the wafer temperature. Thermal stress usually provides a small compressive contribution which is neglected compared to the intrinsic stress.

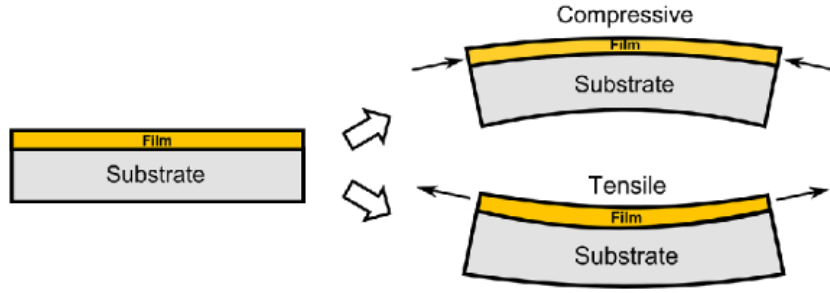


Figure 3.1 - Wafer bow for compressive and tensile stress [19].

Intrinsic stress is related to the bulk of a deposited thin film, i.e. where the film growth is not affected by the substrate surface. This kind of stress depends on complex surface reactions that occur during the deposition process and are strictly related to total pressure and temperature. High total pressure, which means high flow of inert molecules and byproducts, causes a low mobility of reactant species at the surface and so the formation of longer bonds and microcavities. The final result is an increased intrinsic tensile stress. A similar result is achieved for lower temperatures for the same reason discussed above.

The boundary layer has different properties with respect to the bulk film because of the influence of the underlying material. Its properties are dependent on adsorption and reactive species surface mobility. It can be stated that (1) different substrates cause different stress of the boundary layer; (2) the stress of the boundary layer is different from the bulk one. The last statement justifies the fact that if a stressed film is relieved of the constraint of its neighboring substrate, it changes its in-plane configuration due to a stress gradient along the z -axis (see Figure 3.2).

3.2 Bending behavior of a rectangular cantilever

On the basis of what discussed in the previous paragraph, it can be deduced that the unequal surface stresses on both surfaces on a micro-cantilever result in bending [20]. The cantilever bending with a uniform curvature radius can be described by the Stoney's formula [21]. In this approach, the cantilever curvature is the result of a concentrated moment applied at the free end of the micro-cantilever. The bending moment is related to the curvature by:

$$\frac{1}{R} = \frac{M}{E I} \quad (3.4)$$

where E is the Young's modulus and I is the moment of inertia that for a rectangular cross-section is given by:

$$I = \frac{1}{12} w h^3 \quad (3.5)$$

for which w is the cantilever width and h is the beam thickness. The bending moment of the beam caused by the differential in surface stress is:

$$M = \frac{1}{12} w h^3 \Delta\sigma \quad (3.6)$$

where $\Delta\sigma = \sigma_1 - \sigma_2$ is the differential surface stress with σ_1 and σ_2 being surface stresses at the upper and lower surfaces of the cantilever, respectively. Substituting I and M into the Eq. 3.4 is obtained:

$$\frac{1}{R} = \frac{\Delta\sigma}{E} \quad (3.7)$$

From the last formula, it can be deduced that the curvature of a deflected cantilever is directly proportional to the stress gradient measured along the vertical direction z and it is independent on the geometrical lengths of the cantilever.

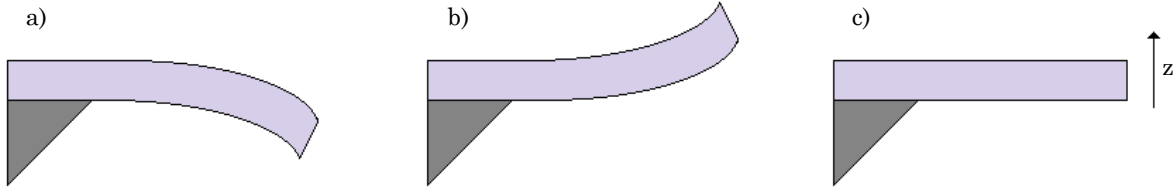


Figure 3.2 - Cantilever deflection induced by different stress gradients along z-direction. a) Higher compressive stress near the cantilever top surface before release from substrate ($\Delta\sigma < 0$). b) Higher tensile stress near the cantilever top surface before release from substrate ($\Delta\sigma > 0$). c) No cantilever bending because there is no stress gradient along z-direction.

3.3 Measurements

The deflection measurements are performed on cantilevers of different lengths and widths but same thickness fabricated on ten wafers. These wafers differ in the recipe used to deposit the silicon nitride thin film on both sides. In particular:

- two <100> DSP wafers are deposited according to HS (High Stress) and LS (Low Stress) CMi recipes and processed following the first process flow with KOH etching at 60°C;
- eight <100> SSP wafers are deposited according to the recipes studied in the previous work [1] and processed using the second process flow.

The deflection of such devices is detected using Veeco Wyko NT100, an optical 3D profiler based on the optical interferometry principle. The operation mode is the same one used for the characterization of the ARDE effect in Section 2.2.3.

Since a complete census data is not feasible, only a subset of twenty cantilevers is studied for each wafer. The data are selected and exported to files through Vision32[®] software which also acts as graphical interface for the optical profiler. At this point, the input files are elaborated by Matlab[®], whose script is reported in Appendix B.

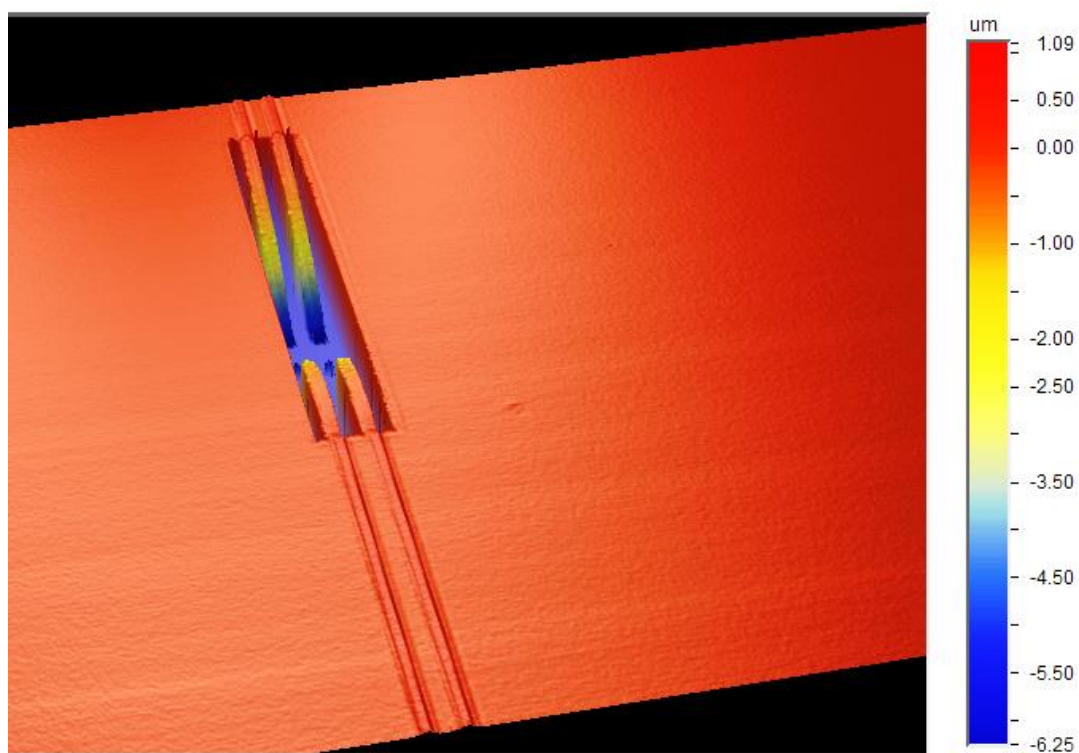


Figure 3.3 - 3D surface profile for a cantilever bending downward.

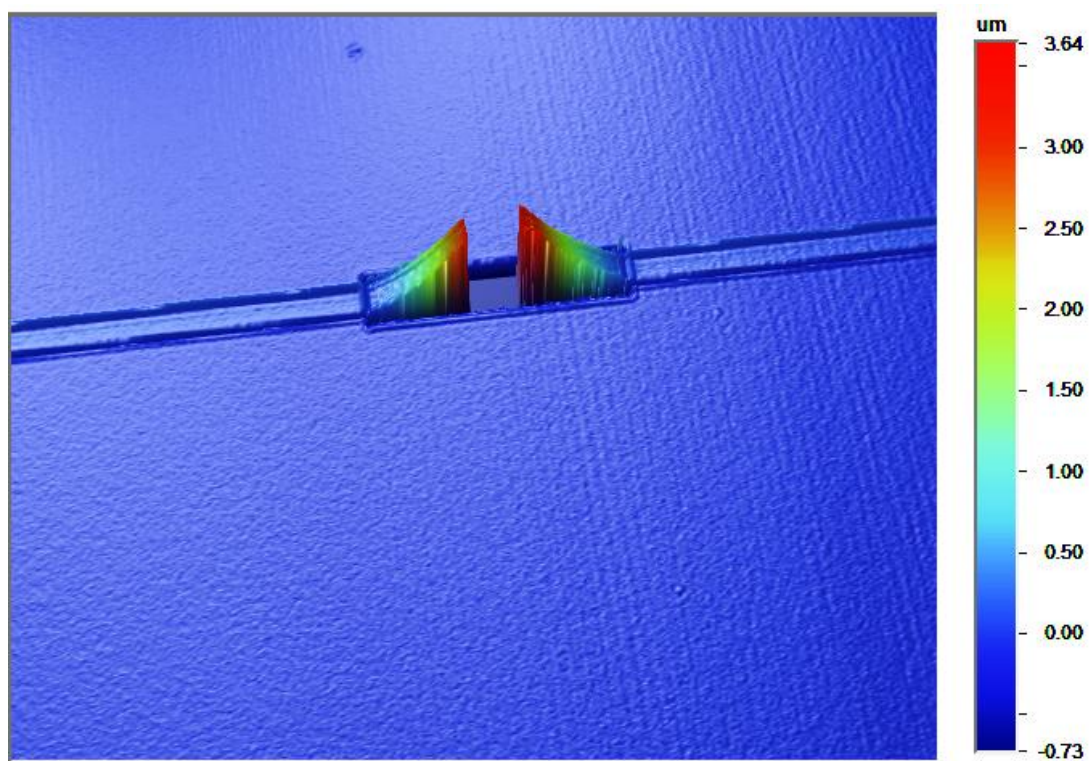
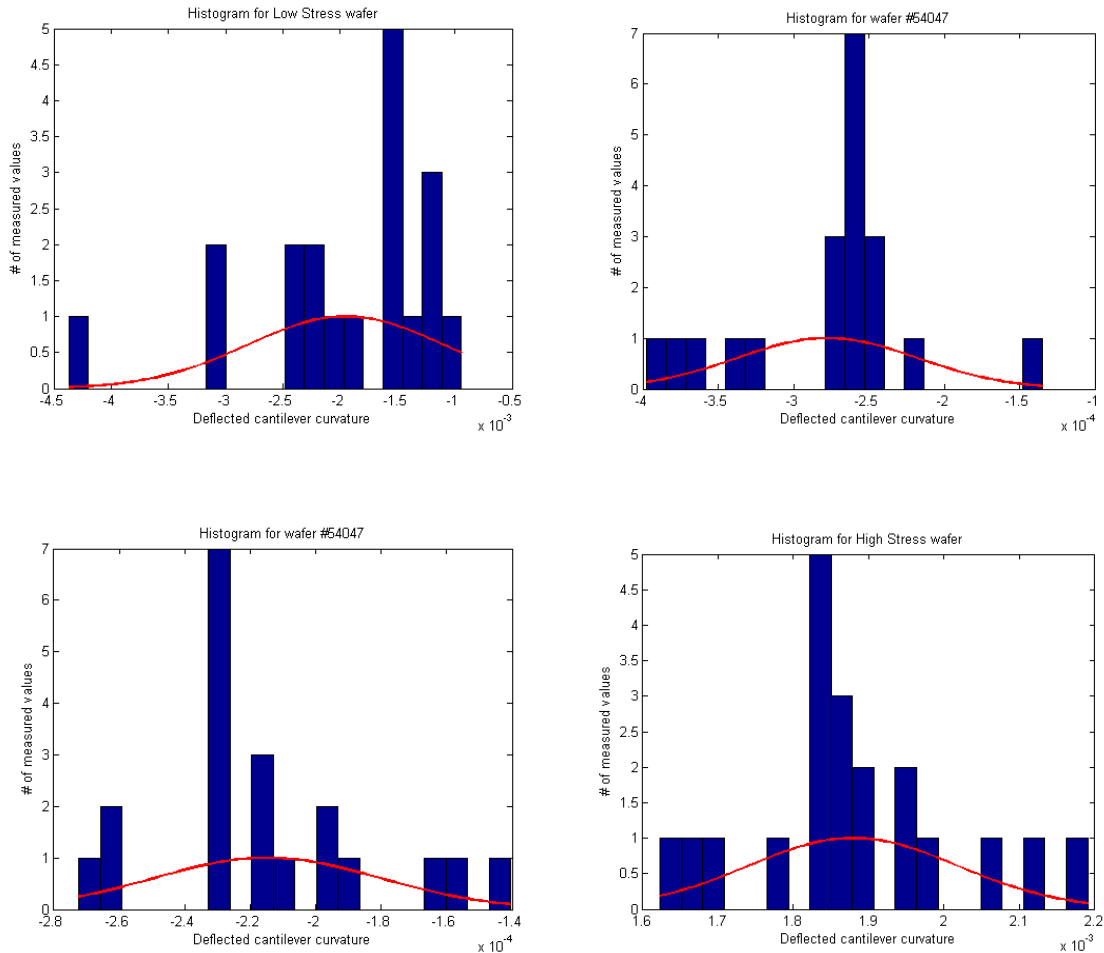
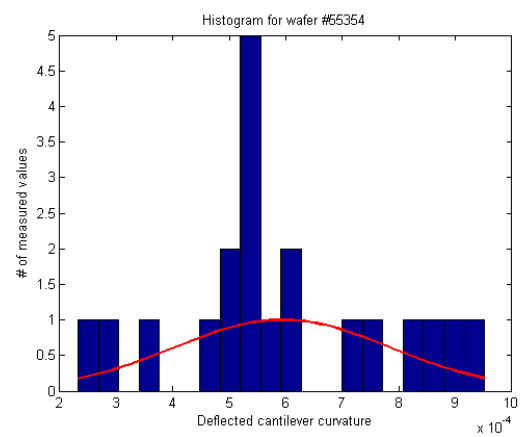
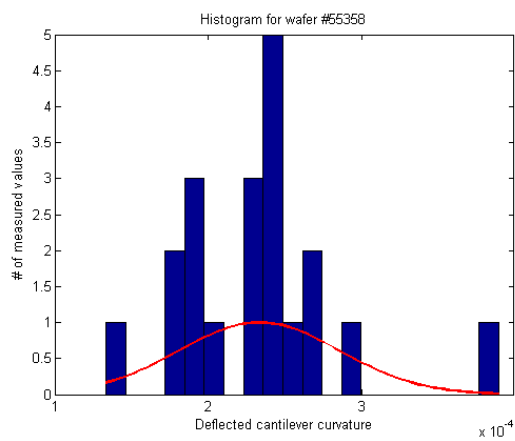
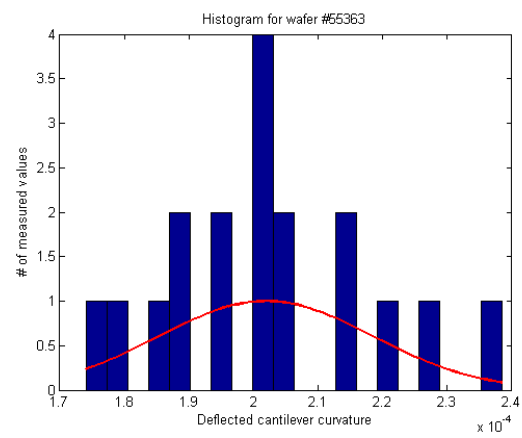
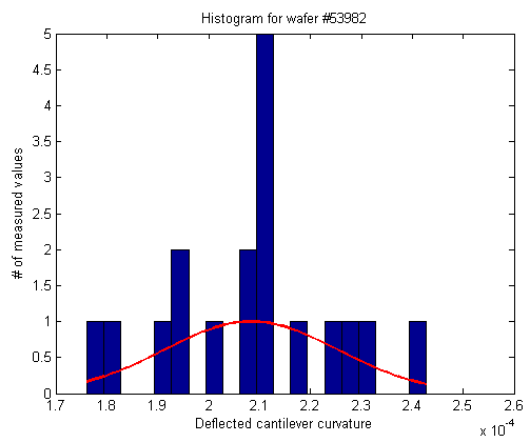
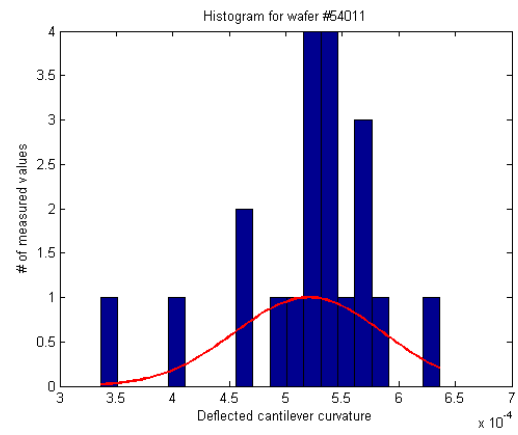
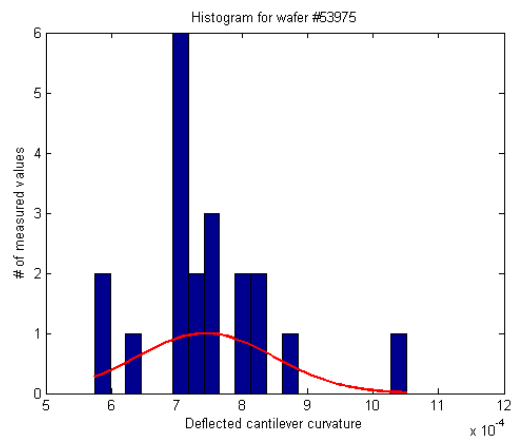


Figure 3.4 - 3D surface profile for a cantilever bending upward.

The numerical values of cantilever curvatures are evaluated starting from the interpolation of the deflection profile, obtained from the interferometric analysis, with a second-order polynomial. Under the assumption of small deflection, the curvature of the deflected cantilever can be approximated as the second order derivative of the deflection profile. For a quadratic function this value is given by $2a$, where a is the coefficient of the second order term.

The measurements obtained for each wafer are grouped in the following histograms, while the mean value, the standard deviation and the variation coefficient are provided in Table 3.1. The variation coefficient is given by the ratio between the standard deviation and the mean value and provides an indication of the variability of the detected observations. In particular, if this ratio is less than 0.5, the mean value is a good indicator.





Wafer number	Recipe	Curvature Mean Value (μm^{-1})	Standard Deviation	Variation coefficient
High Stress	High Stress CMI	0.001879	0.000139	0.074184
#53975	Hmu1	0.000744	0.000105	0.141373
#55354	Hmu8	0.000594	0.000193	0.324455
#54011	Hmu4	0.000520	0.000065	0.125129
#55358	Hmu7	0.000233	0.000053	0.225551
#53982	Hmu5	0.000208	0.000017	0.081830
#55363	Hmu6	0.000202	0.000016	0.081430
#53057	Hmu9	-0.000215	0.000034	0.159976
#54047	Hmu2	-0.000278	0.000060	0.215875
Low Stress	Low Stress CMI	-0.002051	0.000907	0.442030

Table 3.1 - Mean values of curvature measured for ten different recipes. The data are tabulated by decreasing the curvature.

The data listed in the table above are associated to ten different recipes whose details on process parameter and intrinsic material properties can be found in Table 2 Chapter 3 of [1]. According to the data, the curvature can assume positive or negative values. When it is negative the deflected cantilever bends downward because the compressive stress contribution is prevailing. This behavior is verified for low stress silicon nitride thin films deposited at lower temperatures and lower total gas flow. On the other hand, upward bending is measured when a positive stress gradient arises along the thin film thickness. The stress of the upper surface of the cantilever is tensile. In this case, the highest curvature is measured for the “High Stress” recipe prepared by CMI facility and decreases as the deposition process temperature is lowered.

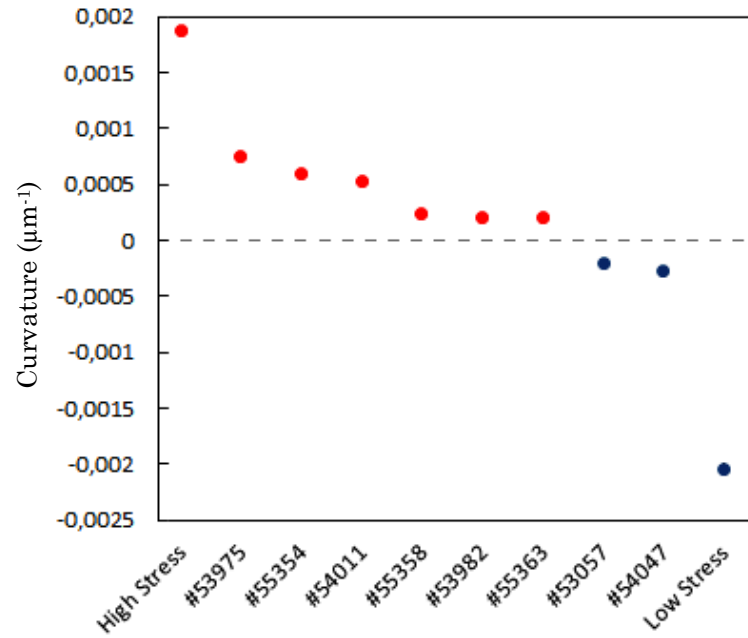


Figure 3.5 - Plot of the measured curvature values for ten different wafers.

By reversing Eq. 3.7 it is possible to estimate the stress gradient along the film thickness using the measured curvature values:

$$\Delta\sigma = \frac{1}{R} E \quad (3.8)$$

The value of the Young's modulus E is taken from [22] as the average between the maximum and minimum values that silicon nitride can assume ($E = 231$ GPa). The following stress gradients are obtained:

Wafer number	Recipe	Stress gradient (GPa/μm)	Stress gradient for 200nm (MPa)
High Stress	High Stress CMi	0.43	96
#53975	Hmu1	0.17	34
#55354	Hmu8	0.14	28
#54011	Hmu4	0.12	24
#55358	Hmu7	0.054	10.8

#53982	Hmu5	0.048	9.6
#55363	Hmu6	0.047	9.4
#53057	Hmu9	-0.050	-10
#54047	Hmu2	-0.064	-12.8
Low Stress	Low Stress CMI	-0.47	-94

Table 3.2 - Calculated stress gradient values for ten different recipes. The Young's modulus is assumed to be 231 GPa. In the last column the stress gradient assuming a film thickness of 200nm has been calculated.

4 Conclusion

The aim of this thesis is to present a method to model, fabricate and characterize silicon nitride nanomechanical resonators. Despite the issues encountered at the beginning of the fabrication, first of all that relative to membranes indentations, the process flow has been significantly optimized in terms of yield and devices quality. Once optimized the process flow, it has been replicated for several wafers which differ from each other to be covered by thin films of silicon nitride with different intrinsic properties. At this point, both static and dynamic mode analysis of devices can be carried out. Due to time constraints, only a static analysis of cantilevers deflection was discussed this time. The first results showed how low stress in silicon nitride thin films lead to compressive stress domain which should be avoided.

4.1 Future perspectives

Most of the time was spent for devices microfabrication and so only measurements in static mode of cantilevers deflection were performed. Dynamic analysis of nanomechanical resonators is vital to assure design and production quality. Thus, the next goal of this project is to conduct a characterization of out-of-plane vibrational behavior of such devices through Scanning Laser Vibrometry. Then the results obtained from experimental measurements will be compared to those derived from analytical formulas and FEM simulations in Ansys®.

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Appendices

A Fabrication details

This appendix contains all the details for the fabrication of silicon nitride nanomechanical resonators at the CMi facility at EPFL. The run sheet for the first fabrication run is presented in Table A.1 while for the second run in Table A.2. Table A.3 contains the detailed process flow of the chrome mask fabrication.

Run sheets are presented assuming that the fabrication is performed on Ø100mm Single Side Polished (SSP) <100> p-type test wafer (0.1-100Ωcm) with 200nm of LPCVD Silicon Nitride deposited on both sides. All parameters listed in the following tables are indicative and valid only for the time when the process has been performed. Since many tools periodically undergo maintenance, it is strongly recommended to:

- check the exposure parameters through exposure tests for all lithography steps. For this purpose, the design shown in Fig. 2.5 c can be used.
- characterize the etch rate for each etch process on a dummy wafer. As regards wet etching, check using the labelled densimeter that the density at room temperature of the KOH bath at 60°C is 1.39 before heating and pumping the system. Before starting the Bosch process on ALCATEL 601E, it is recommended to launch the recipe “Si_release” for 5 minutes to clean the chamber from residuals of previous processes.
- check that the name of the recipes is not changed.

FIRST FABRICATION RUN

STEP	DESCRIPTION	TOOL	RECIPE, PARAMETERS AND NOTES
0.x	Wafer preparation		
0.1	Stock out		-
0.2	Check wafer thickness	Nanospec AFT-6100	-
1.x	Photolithography (Back Side)		
1.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry.
1.2	Spin coating	ACS 200 GEN3	Recipe number: 0123. Bake, HexaMethylDiSilazane (HMDS) and post bake. Edge Bead Removal (EBR) not needed. Resist type: AZ ECI 3007, thickness 1 μm .
1.3	Exposure	Heidelberg VPG200	Dose: 90mJ/cm ² , write head: 20mm
1.4	Development	ACS 200 GEN3	Recipe number: 0923. Development and hard baking.
1.5	Spin rinser dryer	Semitool	Mandatory step to avoid cross contamination with the equipment.
1.6	Optical inspection	Nikon Optiphot 200	-
2.x	Dry etching		
2.1	Si ₃ N ₄ dry etching	SPTS APS Dielectric Etcher	Recipe: 'Si ₃ N ₄ Smooth'. Duration: 2 min.
3.x	Resist strip		
3.1	Dry strip in oxygen plasma	Tepla GiGAbatch	Program: PR_Strip_Low_1min. Note: this step is mandatory to remove the top burned PR layer.
3.2	Wet strip 1 st bath	Ultrafab wetbench	Bath filled with Remover 1165 at 70°C. Duration: 5m.
3.3	Wet strip 2 nd bath	Ultrafab wetbench	Bath filled with Remover 1165 at 70°C. Duration: 5m.
3.4	Rough rinsing	Ultrafab wetbench	Quick Dump Rinse (QDR).

3.5	Fine rinsing	Ultrafab wetbench	Cascade Tank (CT).
3.6	Drying	Semitool	Program 2. Dry wafer.
4.x	Wet etching		
4.1	Bath heating	Plade Six Sigma	The bath density at 90°C is 1.18.
4.2	Si wet etching	Plade Six Sigma	Etching duration: 4h 15m.
4.3	Rough rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
4.4	Fine rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
4.5	Neutralization	Plade Six Sigma	Neutralization in HCl 37% bath. Duration: 2h.
4.6	Rough rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
4.7	Fine rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
4.8	Optical inspection	Nikon Optiphot 200	-
5.x	Wafer sticking		
5.1	Sticking	RC8 THP Hot Plate	Wax: QuickStick135. Program n°19. Hot plate temperature: 135°C.
6.x	Photolithography (Front Side)		
6.1	Spin coating	ACS 200 GEN3	Recipe number: 0301. Bake, HexaMethylDiSilazane (HMDS) and post bake. Edge Bead Removal (EBR) is needed. Resist type: AZ1512, thickness 1.1 µm.
6.2	Mask alignment and exposure	Süss MA6 GEN3	Exposure mode: Proximity. Exposure time: 2s.
6.3	Development	ACS 200 GEN3	Recipe number: 0901. CMiDev.AZ1512 1µm16.puddle. Development and hard baking.
6.4	Optical inspection	Nikon Optiphot 200	-
7.x	Dry etching		
7.1	Si ₃ N ₄ dry etching	SPTS APS Dielectric Etcher	Recipe: 'Si ₃ N ₄ Smooth'. Duration: 2 min.

8.x	Resist strip		
8.1	Dry strip in oxygen plasma	Oxford PRS900	Program: Strip_oxygen_40min. Power: 1000W.
9.x	QuickStick135 removal		
9.1	Wafer separation	RC8 THP Hot Plate	Program n°19. Hot plate temperature: 135°C.
9.2	Wafer cleaning	Miscellaneous wet bench	Cleaning with Acetone.

Table A.1 - Detailed run sheet for the first fabrication run at the CMi facility.

SECOND FABRICATION RUN

STEP	DESCRIPTION	TOOL	RECIPE, PARAMETERS AND NOTES
0.x	Wafer preparation		
0.1	Stock out		-
0.2	Check wafer thickness	Nanospec AFT-6100	-
1.x	Si DC Sputtering (Front Side)		
1.1	Chamber cleaning	Pfeiffer SPIDER 600	Recipe: Si_C-1.
1.2	Amorphous Si Deposition	Pfeiffer SPIDER 600	Recipe: Si-1. Layer thickness: 200nm. Deposition time: 2m 4s.
2.x	Photolithography (Back Side)		
2.1	Spin rinser dryer	Semitool	Program 1. Rinse wafer and dry.
2.2	Spin coating	ACS 200 GEN3	Recipe number: 0129. Bake, HexaMethylDiSilazane (HMDS) and post bake. Edge Bead Removal (EBR) not needed. Resist type: AZ ECI 3027, thickness 5 μm .
2.3	Exposure	Heidelberg VPG200	Dose: 360mJ/cm ² , write head: 5mm
2.4	Development	ACS 200 GEN3	Recipe number: 0929. Development and hard baking.
2.5	Spin rinser dryer	Semitool	Mandatory step to avoid cross contamination with the equipment.
2.6	Optical inspection	Nikon Optiphot 200	-
2.7	Overnight bake	Heraeus Thermo Scientific Oven	Baking at 80°C for all the night.
3.x	Dry etching		
3.1	Si ₃ N ₄ dry etching	SPTS APS Dielectric Etcher	Recipe: 'Si ₃ N ₄ Smooth'. Duration: 2 min.

4.x	Dry etching (Bosch Etching)		
4.1	Thermalization	ALCATEL 601E	Program: THERM +20°C.
4.2	Si Dry Etching	ALCATEL 601E	Recipe: Si_AMBIANT2. Duration: 45m.
4.3	Optical inspection	Veeco Wyko NT1100	Checking up of the trenches depth..
5.x	Resist strip		
5.1	Dry strip in oxygen plasma	Tepla GiGAbatch	Program: PR_Strip_High_5min.
6.x	Wet etching		
6.1	Bath heating	Plade Six Sigma	The bath density at 60°C is 1.39.
6.2	Si wet etching	Plade Six Sigma	Etching duration: 5h.
6.3	Rough rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
6.4	Fine rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
6.5	Neutralization	Plade Six Sigma	Neutralization in HCl 37% bath. Duration: 2h.
6.6	Rough rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
6.7	Fine rinsing	Plade Six Sigma	Fast Fill Rinse (FFR). Duration: 5m.
6.8	Optical inspection	Nikon Optiphot 200	-
7.x	Wafer sticking		
7.1	Sticking	RC8 THP Hot Plate	Wax: QuickStick135. Program n°19. Hot plate temperature: 135°C.
8.x	Photolithography (Front Side)		
8.1	Spin coating	ACS 200 GEN3	Recipe number: 0301. Bake, HexaMethylDiSilazane (HMDS) and post bake. Edge Bead Removal (EBR) is needed. Resist type: AZ1512, thickness 1.1 µm.
8.2	Mask alignment and exposure	Süss MA6 GEN3	Exposure mode: Proximity. Exposure time: 2s.
8.3	Development	ACS 200 GEN3	Recipe number: 0901. CMiDev.AZ1512 1µm16.puddle. Development and hard baking.

8.4	Optical inspection	Nikon Optiphot 200	-
9.x	Dry etching		
9.1	Si ₃ N ₄ dry etching	SPTS APS Dielectric Etcher	Recipe: 'Si ₃ N ₄ Smooth'. Duration: 2 min.
10.x	Resist strip		
10.1	Dry strip in oxygen plasma	Oxford PRS900	Program: Strip_oxygen_40min. Power: 1000W.
11.x	QuickStick135 removal		
11.1	Wafer separation	RC8 THP Hot Plate	Program n°19. Hot plate temperature: 135°C.
11.2	Wafer cleaning	Miscellaneous wet bench	Cleaning with Acetone.

Table A.2 - Detailed run sheet for the second fabrication run at the CMi facility.

MASK FABRICATION

STEP	DESCRIPTION	TOOL	RECIPE, PARAMETERS AND NOTES
0.x	Mask preparation		
0.1	Stock out		-
1.x	Photolithography		
1.1	Exposure	Heidelberg VPG200	Intensity: 35%, write head: 20mm.
1.2	Development	Süss DV10	Recipe: Cr blank 5P fine. Note: Developers purge is recommended before starting the process.
1.3	Optical inspection	Nikon Optiphot 200	-
2.x	Wet etching		
2.1	Cr wet etching	Coillard Etching – Wet bench	Commercial bath CR1. Etching time: 90s.
2.2	Rough rinsing	Coillard Etching – Wet bench	Quick Dump Rinse.
2.3	Fine rinsing	Coillard Etching – Wet bench	Ultra-Clean Cascade Tank.
2.4	Drying	Manual	N ₂ gun.
3.x	Resist strip		
3.1	Wet strip	Coillard Photo	Technistrip P1316 bath. Duration: 10m.
3.2	Rough rinsing	Coillard Photo	Quick Dump Rinse.
3.3	Fine rinsing	Coillard Photo	Ultra-Clean Cascade Tank.
3.4	Drying	Manual	N ₂ gun.
3.5	Optical inspection	Nikon Optiphot 200	-

Table A.3 - Detailed run sheet for the chrome mask fabrication at the CMi facility.

B Matlab code

In this appendix the Matlab script used for the cantilever curvature characterization is presented.

```

1  % Matlab script for the evaluation of the deflected cantilevers curvature.
2  % Alberto Barulli 29.08.2016
3
4  clear all
5  format long;
6
7  N=20;                                %% Number of measurements taken for each wafer
8  gamma=zeros(1,N);
9
10 for k=1:N
11     A=load(strcat('DATA',num2str(k),'.txt'));           %%Automatic files loading
12     X=A(:,1)-A(1,1);                                     %% Shifting of data to the origin of the axes
13     Y=A(:,2)-A(1,2);                                     %% Shifting of data to the origin of the axes
14     P=polyfit(X, Y, 2);
15     gamma(k)=P(1)*2;  %% Evaluation of the curvature of the deflected cantilever
16     x=linspace(0, X(length(X)), 100);
17     y=polyval(P, x);
18     figure
19     plot(X, Y, 'b.')
20     hold on
21     plot(x, y, 'r','LineWidth',2)
22 end
23
24 gamma
25 M=mean(gamma);                                           %% Evaluation of the mean
26 STD=std(gamma);                                         %% Evaluation of the standard deviation
27 R=abs(STD/M);                                           %% This parameter should be <0.5 for a good sampling
28
29 figure
30 hist(gamma,20)
31 title('Histogram for wafer #55354')

```

```
32 xlabel('Deflected cantilever curvature')
33 ylabel('# of measured values')
34
35 fprintf('The mean value is: %f \n', M);
36 fprintf('The standard deviation is: %f \n', STD);
37 fprintf('The ratio STD/M is: %f \n', R);
```

Acronyms

MEMS Micro ElectroMechanical Systems.

NEMS Nano ElectroMechanical Systems.

EPFL Ecole Polytechnique Fédérale de Lausanne.

AFM Atomic Force Microscope.

RF Radio Frequency.

CMi Center of Micronanotechnology.

SEM Scanning Electron Microscope.

DRIE Deep Reactive Ion Etching.

RIE Reactive Ion Etching.

FEM Finite Element Modelling.

SSP Single Side Polished.

LPCVD Low Pressure Chemical Vapor Deposition.

DSP Double Side Polished.

ARDE Aspect Ratio Dependent Etch.

AR Aspect Ratio.

VSI Vertical Scanning Interferometry.

EBR Edge Bead Removal.

HMDS HexaMethylDiSilazane.

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